Abstract of the Disclosure

In a frequency multiplier and a method of multiplying a frequency of an external clock signal, a data output buffer, and a semiconductor device including the frequency multiplier and the data output buffer, the frequency multiplier receives an external clock signal having a predetermined frequency and outputs an internal clock signal having greater frequency than the predetermined frequency. In the semiconductor device, the data output buffer outputs data tested in response to test data. Therefore, it is possible to test a plurality of memory cells at a time by using a clock signal having a low frequency. In addition, the time and cost required for the test can be greatly reduced, and conventional testing equipment that operates at a relatively low frequency can be effectively used.

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